# A 130 nm Generation Logic Technology Featuring 70nm Transistors, Dual Vt Transistors and 6 layers of Cu Interconnects

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**Abstract**

A leading edge 130 nm generation logic technology with 6 layers of dual damascene Cu interconnects is reported. Dual Vt transistors are employed with 1.5 nm thick gate oxide and operating at 1.3 V. High Vt transistors have drive currents of 1.03 mA/μm and 0.5 mA/μm for NMOS and PMOS respectively, while low Vt transistors have currents of 1.17 mA/μm and 0.6 mA/μm respectively. Technology design rules allow a 6-T SRAM cell with an area of 2.45 $\mu m^2$, while array specific design rule give the densest SRAM reported to date, the 6-T cell has an area of only 2.09 $\mu m^2$. Excellent yield and performance is demonstrated on a 18 Mbit CMOS SRAM.

## Introduction

High performance microprocessors require faster transistors operating at lower voltages to maintain the historic speed trend at acceptable active power. In this paper we describe a 130 nm generation technology operating at 1.3V for high speed and low power operation. Transistor leakage in off state is another concern, which constrains chip performance as it affects standby power. Dual threshold voltages are offered for both NMOS and PMOS transistors to improve product performance at acceptable standby leakage. Increasingly the circuit speed is also being affected by performance of interconnects. The technology uses 6 layers of dual damascene Cu with fluorinated $SiO_2$ for high performance interconnects.

## Process flow and front end technology features

The technology features are summarized in Table I below giving layer pitches and thicknesses. Fig. 1 shows a cross-sectional TEM for a transistor with 70nm gate length.

TABLE I
LAYER PITCH, THICKNESS AND ASPECT RATIO

| Layer | Pitch (nm) | Thick (nm) | Aspect Ratio |
|---|---|---|---|
| Isolation | 364 | 450 | |
| Poly-silicon | 336 | 160 | |
| Metal 1 | 350 | 280 | 1.6 |
| Metal 2, 3 | 448 | 360 | 1.6 |
| Metal 4 | 756 | 570 | 1.5 |
| Metal 5 | 1120 | 900 | 1.6 |
| Metal 6 | 1204 | 1200 | 2.0 |

The process flow starts with P-/P+ epitaxial silicon wafers, followed by the formation of shallow trench isolation. N-wells and P-wells are formed with deep phosphorous and shallow arsenic implants, and boron implants respectively. The trench isolation is 450 nm deep to provide good intra- and inter-well isolation. Fig. 2 shows that isolation is robust for N+ to P+ spacing below 300 nm.

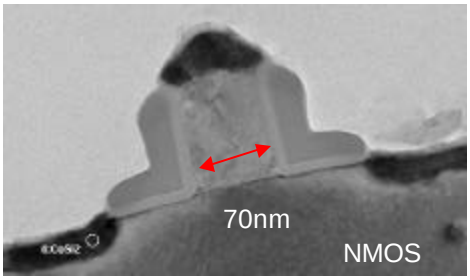
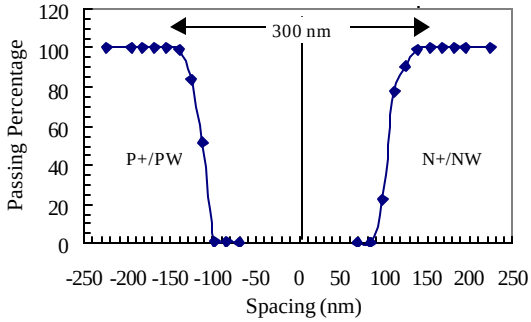



**Fig.1** TEM Cross–section of a 70 nm NMOS transistor.
**Fig. 2** Percentage passing electrical isolation criteria for N+/NW and P+/PW spacing.




High quality gate oxide is then grown, the physical thickness of the oxide is 1.5 nm. Complementary-doped poly-silicon is used to form surface-channel NMOS and PMOS devices. DUV lithography is used to pattern the poly-silicon gate layer down to gate dimension of 70 nm as shown in Fig. 1. Shallow source-drain extensions regions are formed with arsenic for NMOS and boron for PMOS. Boron and arsenic halos are used in both cases for improved short channel characteristics. Side-wall spacers are formed with CVD $Si_3N_4$ deposition, followed by etch-back. $CoSi_2$ is formed on poly-silicon and source-drain regions to provide low contact resistance.

## Transistors

To improve product performance at acceptable standby leakage, NMOS and PMOS devices with high and low

threshold voltages are made by selectively adjusting well doses. The transistor characteristics are shown in Figs. 3 and 4 for high and low threshold devices respectively. Saturation drive currents for high Vt devices at Ioff value of 10 nA/μm, are 1.03 mA/μm for NMOS and 0.5 mA/μm for PMOS. For low Vt devices the Ioff is 100 nA/μm, and the currents are 1.17 mA/μm for NMOS and 0.6 mA/μm for PMOS.

**Fig. 3** High Vt MOSFET Id-Vd characteristics.

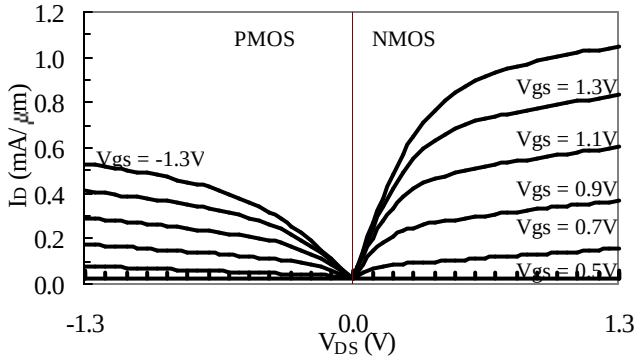
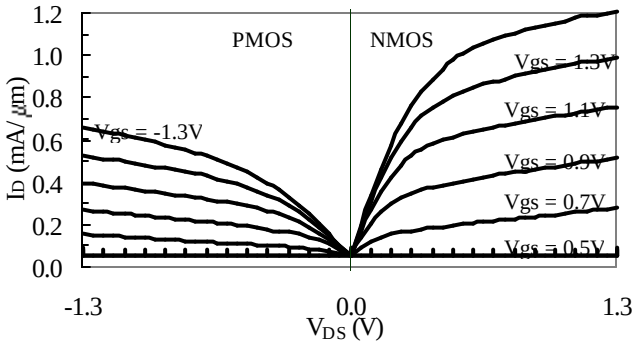
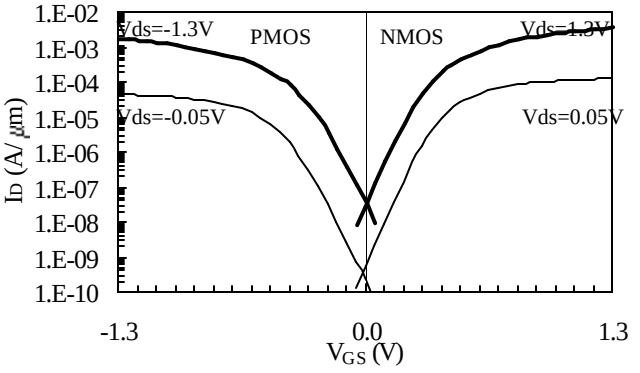



**Fig. 4** Low Vt MOSFET Id-Vd characteristics.



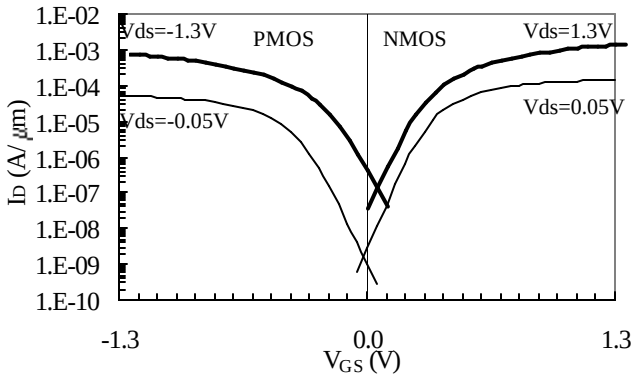

The subthreshold slopes for these devices are shown in Fig. 5 and 6 and are less than 95 mV/decade.

**Fig. 5** High Vt subthreshold characteristics.




The DIBL for the 70 nm NMOS device is measured to be 100 mV/V for high Vt devices and 110 mV/V for low Vt device. For the PMOS device the measured DIBL is 100 mV/V for high Vt device and 130 mV/V for low Vt device.

**Fig. 6** Low Vt subthreshold characteristics.




The NMOS and PMOS drive current vs. off current characteristics are shown in Fig. 7 for both the high and low Vt devices. These are the best Ion-Ioff characteristics reported to date.

**Fig. 7** Drive current vs. off current for NMOS and PMOS. Unfilled symbols are high Vt devices, while filled symbols are low Vt devices.

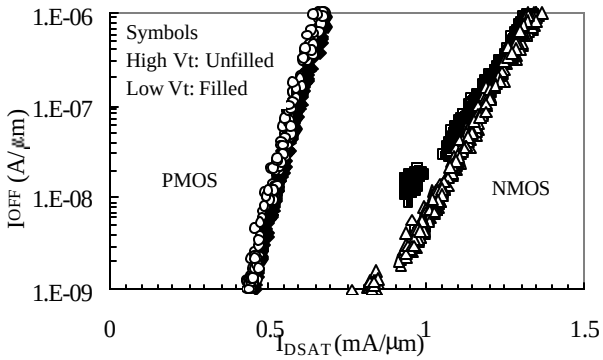



Table II compares the transistor characteristics in this work to those reported earlier by our group [1].

TABLE II
SUMMARY OF TRANSISTOR CHARACTERISTICS

| Parameter | | 180 nm Generation [1] | This Work |
|---|---|---|---|
| $V_{DD}$ | [V] | 1.5 | 1.3 |
| $L_{GATE}$ | [nm] | 130 | 70 |
| $T_{OX}$ | [nm] | 2.0 | 1.5 |
| $I_{OFF}$ | [nA/μm] | 3 | 10 |
| $I_{DSAT}$(n) | [mA/μm] | 1.04 | 1.02 |
| $I_{DSAT}$ (p) | [mA/μm] | 0.46 | 0.5 |
| Low Vt $I_{OFF}$ | [nA/μm] | - | 100 |
| Low Vt $I_{DSAT}$(n) | [mA/μm] | - | 1.17 |
| Low Vt $I_{DSAT}$ (p) | [mA/μm] | - | 0.6 |

The thin 1.5 nm oxide enables devices with well controlled short channel characteristics down to 70 nm gate lengths.

The threshold voltage roll-off characteristics are shown in Fig. 8 and 9 for high and low Vt devices respectively. Optimal Halo and well engineering gives Vt roll off of less than 100 mV for the target 70 nm devices. This is achieved by using the halo to boost the average well doping for shorter gate length devices. This reduces the magnitude of Vt roll off due to short channel effects.

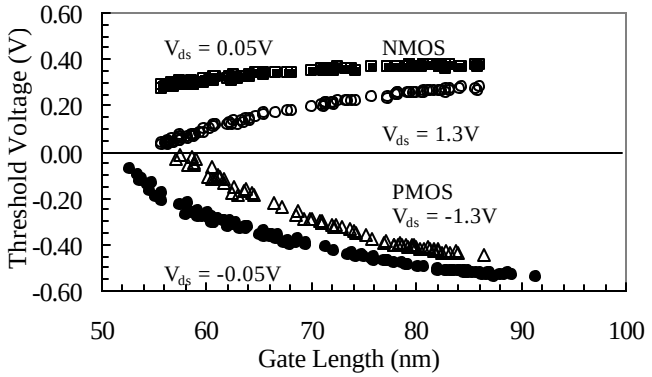



**Fig. 8** Hi Vt threshold voltages vs. gate length.

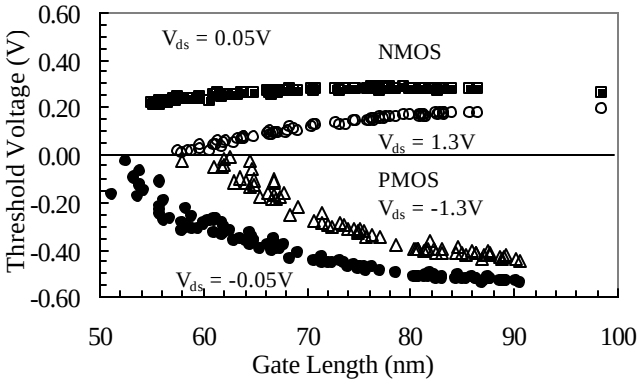
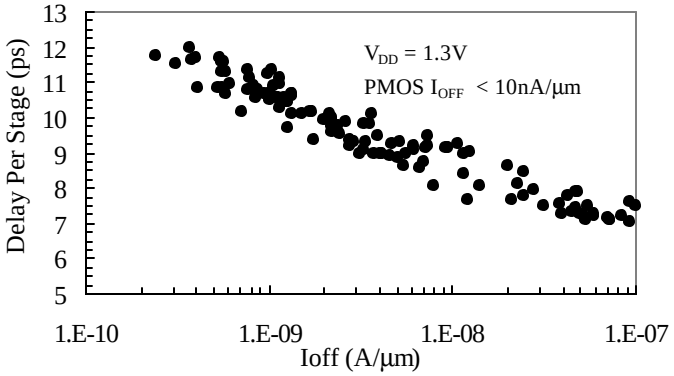



**Fig. 9** Low Vt threshold voltages vs. gate length.

Junction capacitance plays an important role in limiting chip performance and increasing active power. Special emphasis was placed on minimizing junction capacitance values. Low N+ and P+ junction area capacitance values of 0.6 fF/$\mu m^2$ at 0 V bias were achieved while maintaining the intra- and inter-well isolation.

Ring oscillator propagation delays are used to benchmark the performance of the transistors in a circuit configuration. Fig.10 shows the propagation delay per stage of an unloaded ring oscillator as function of NMOS off current, the PMOS off current is less than 10 nA/$\mu$m. The ring oscillator has a fanout of 1 and a $W_p/W_n$ ratio of 1.5, the $V_{DD}$ is 1.3 V and measurements are at room temperature. For the target high Vt device with Ioff 10 nA/$\mu$m, the delay per stage is 8 pico-seconds while for the low Vt device with Ioff 100 nA/$\mu$m, the delay is 7 pico-seconds. These are the best reported values to date.

**Fig. 10** Propagation delay per stage of unloaded ring oscillator with fan out =1 and $W_p/W_n$ ratio of 1.5.




**Interconnects**

Chip performance is increasingly limited by the RC delay of the interconnect as the transistor delay progressively decreases while the narrower lines and space actually increase the delay associated with interconnects [2]. Using copper interconnects helps reduce this effect. This process technology uses dual damascene copper to reduce the resistances of the interconnects. Fluorinated $SiO_2$ (FSG) is used as inter-level dielectric (ILD) to reduce the dielectric constant, the dielectric constant k is measured to be 3.6. Fig. 11 is a cross-section SEM image showing the dual damascene interconnects.

**Fig. 11** Cross-section SEM image of a processed wafer.

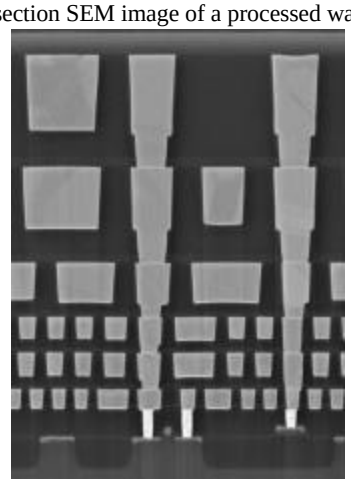
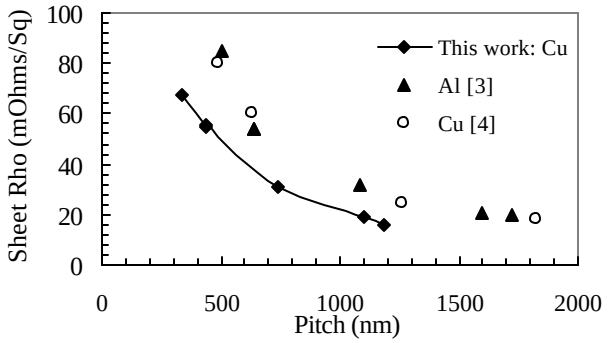


Table I. lists the metal pitches, the pitch is 350 nm at the first metal layer and increases to 1200 nm at the top layer. Metal aspect ratios are optimized for minimum RC delay, and range from 1.6 to 2. The first metal layer uses a single damascene process and tungsten plugs are used as contacts to the silicided regions on the silicon and poly-silicon. Unlanded contacts are supported by using a $Si_3N_4$ layer for contact etch stop. Copper interconnects are used because of the material's lower resistivity. The advantage is seen in Fig. 12, where the sheet resistance is shown as a function of the minimum pitch of each metal layer and compared to earlier results from 180nm technologies using Al [3] and Cu [4]. The present technology exhibits 30% lower sheet resistance at the same metal pitch due to the use of Cu with high aspect ratios.

The total line capacitance is 230 fF/mm for M1 to M5 and slightly higher for M6.

**Fig. 12** Sheet resistance as a function of layer pitch.

To benchmark the performance of interconnects, Fig. 13 shows the RC delay in picoseconds per millimeter of wire.

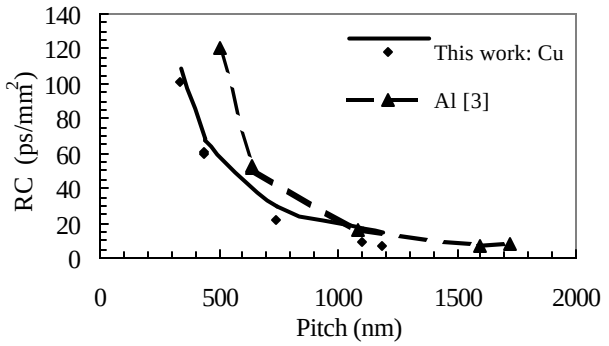



Data for each metal layer is shown as a function of the minimum pitch at that layer. For a given pitch, 40% reduction in RC is achieved by using Cu interconnects and FSG ILD.

**Fig. 13** RC delay for a wire length of 1mm as a function of layer pitch.

## SRAM Yield and Performance

A 18 Mbit CMOS SRAM [5] was shrunk to technology




design rules, the shrunk die size is 103 $mm^2$. This SRAM is used as a yield and reliability test vehicle during the process development and to test and refine the SRAM cell and support circuitry to be used in logic products. The technology features enable a 2.45 $\mu m^2$ 6-T SRAM cell (1.4 μm x 1.75 μm) without the using a local interconnect layer. Array specific design rules allow a smaller 2.09 $\mu m^2$ 6-T SRAM cell (1.23 μm x 1.69 μm), this is the densest reported cell to date. Fig. 14 shows a top down SEM of the active areas and polysilicon gate for both these cells. The SRAM die yield is equivalent to past technologies at this point of time relative to ramping in high volume manufacturing.

The SRAM performance is measured using its Fmax. Fig. 15 shows the schmoo plot for the SRAM, i.e. the Fmax is shown as a function of voltage. The tester capability presently limits the Fmax measurement to 1.6GHz. As is seen in Fig. 15, at 1.3V the SRAM operates at clock period of 0.625ns, or Fmax of 1.6Ghz.

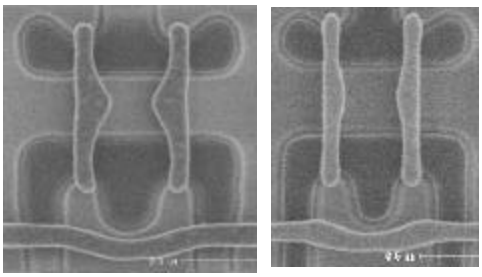
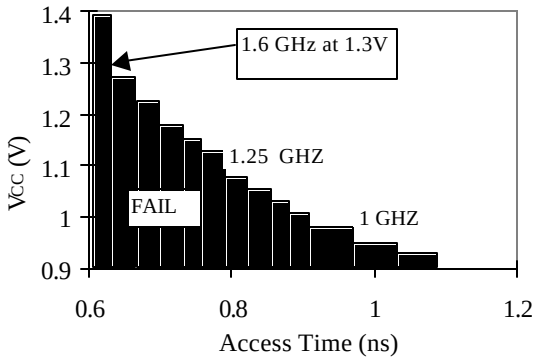


**Fig. 14** Top down SEM of the 2.45 $\mu m^2$ 6-T SRAM bit cell on left and the 2.09 $\mu m^2$ 6-T SRAM on right.

**Fig. 15** Fmax schmoo plot for 16Mbit SRAM.

## Conclusion

A 130 nm generation logic technology has been demonstrated with low power high performance transistors.




Excellent interconnect performance is achieved by using 6 layers of dual damascene Cu with FSG dielectrics. The technology performance capabilities are demonstrated with ring oscillator delays of 7 ps/stage and with a 18 Mbit SRAM operating at 1.6 MHz.


## Acknowledgement

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